

a junction unit for changing the state of a junction formed between the connection terminals and the wiring pattern, wherein the junction unit includes at least one of a dip switch for switching a junction between each of a plurality of wiring patterns and a single connection terminal, and a dip switch for switching a junction between a plurality of connection terminals and a single wiring pattern.

Please add new claim 12.

--12. The inspection apparatus according to claim 10, wherein the junction unit includes a pin socket for connecting the wiring pattern to the connection terminals when a pin is inserted into the pin socket, and the pin socket is interposed between each of a plurality of wiring patterns and a single connection terminal and/or between each of a plurality of connection terminals and a single wiring pattern.--

REMARKS

This Amendment is being filed in response to the Office Action dated January 30, 2002. For the following reasons, this Application should be considered in condition for allowance and the case passed to issue.

Initially, it is noted that no extension of time fee is required for this amendment to be entered because a Shortened Statutory Period For Reply was not set in this application (See attached Office Action Summary).

No new matter is introduced by these amendments. The corrections to the specification merely clarify informalities. The amendments to claim 8 are supported by originally filed claim 7, the specification at page 14, line 27 to page 15, line 6, and FIG. 5 and 6. The amendments to claims 9 and 10 are supported by originally filed claim 7. New claim 12 is supported by originally filed claim 8.

Specification

The specification is objected to because of several informalities. These informalities have been corrected by this amendment.

Claim Rejections Under 35 USC § 102(b)

Claims 7-11 are rejected under 35 USC § 102(b) as being anticipated by Tada et al. (U.S. Patent No. 4,801,871). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison of the invention as claimed with the cited prior art.

An aspect of the invention, per claim 8, is an inspection apparatus for inspecting a plurality of semiconductor integrated circuits mounted on a base board. The base board comprises a plurality of connection terminals electrically connected to terminals of an inspection main unit and a plurality of wiring patterns connected to terminals of a semiconductor integrated circuit. The base board further comprises a junction unit for changing the state of a junction formed between the connection terminals and the wiring pattern. The junction unit includes a group of pin sockets each of which is interposed between each of a plurality of wiring patterns and a single connection terminal and/or a group of pin sockets each of which is interposed between each of a plurality of connection terminals and a single wiring pattern. Each of the pin sockets connects the wiring pattern to the connection terminal when a pin is inserted therein.

Another aspect of the invention, per claim 9, is an inspection apparatus for inspecting a plurality of semiconductor integrated circuits mounted on a base board. The base board comprises a plurality of connection terminals electrically connected to terminals

of an inspection main unit and a plurality of wiring patterns connected to terminals of a semiconductor integrated circuit. The base board further comprises a junction unit for changing the state of a junction formed between the connection terminals and the wiring pattern. The junction unit includes an element mount pattern for connecting the wiring pattern to the connection terminals when a short-circuit element is mounted on the element mount pattern. The element mount pattern is provided between each of a plurality of wiring patterns and a single connection terminal and/or between each of a plurality of connection terminals and a single wiring pattern.

Another aspect of the invention, per claim 10, is an inspection apparatus for inspecting a plurality of semiconductor integrated circuits mounted on a base board. The base board comprises a plurality of connection terminals electrically connected to terminals of an inspection main unit and a plurality of wiring patterns connected to terminals of a semiconductor integrated circuit. The inspection apparatus further comprises a junction unit for changing the state of a junction formed between the connection terminal and the wiring pattern. The junction unit includes at least one of a dip switch for switching a junction between each of a plurality of wiring patterns and a single connection terminals and a dip switch for switching a junction between a plurality of connection terminals and a single wiring pattern.

Another aspect of the invention, per claim 11, is a method for inspecting a semiconductor integrated circuit using an inspection apparatus for inspecting a plurality of semiconductor integrated circuits mounted on a base board. The apparatus comprises a plurality of relay pins electrically connected to a wiring pattern laid on the base board. Sockets are provided on the base board, each housing a semiconductor integrated circuit.

The apparatus further comprises exchange boards, each electrically connecting socket terminals on the socket to a specific relay pin and spacers interposed between each of the exchange boards and the base board.

The Examiner asserts that Tada discloses a plurality of connection terminals (3a-3j) electrically connected to terminals of an inspection main unit (30), a plurality of wiring patterns (40) connected to terminals (1a-1j) of a semiconductor IC (DUT), and a junction unit and (RV1-RG10) for changing the state of a junction formed between the connection terminals and the wiring pattern in FIG. 1. The Examiner further avers that the junction unit includes a pin socket (2) for connecting the wiring pattern to the connection terminals when a pin is inserted into the pin socket, and the pin socket is interposed between each of a plurality of wiring patterns and the single connection terminal and/or between each of a plurality of connection terminals and a single wiring pattern.

As illustrated in FIG. 1 and 6, Tada teaches pins 3a-3j, provided in the pin electronic cards of the tester 3, are connected to the driver D or the comparator C by relays R1 and R2, not by a pin. In contrast thereto, claim 8 requires, as illustrated in FIG. 5 and 6, that a pin socket 44 is connected to a wiring pattern 42 when pin 46 is inserted into the pin socket. The claimed connections of the instant invention are not made through relays, as taught by Tada.

In addition, Tada does not teach the junction unit for changing the state of a junction formed between the connection terminals and the wiring pattern, wherein the junction unit includes a group of pin sockets each of which is interposed between each of a plurality of wiring patterns and a single connection terminal and/or a group of pin sockets each of which is interposed between each of a plurality of connection terminals and a single wiring pattern,

each of the pin sockets connecting the wiring pattern to the connection terminal when a pin is inserted therein, as required by claim 8.

Tada also does not teach an inspection apparatus wherein the junction unit includes an element mount pattern for connecting the wiring pattern to the connection terminals when a short-circuit element is mounted on the element mount pattern, and the element mount pattern is provided between each of a plurality of wiring patterns and the single connection terminal and/or between each of a plurality of connection terminals and the single wiring pattern, as required by claim 9.

In addition, Tada does not disclose the junction unit including at least one of a dip switch for switching a junction between each of a plurality of wiring patterns and a single connection terminal and a dip switch for switching a junction between a plurality of connection terminals and a single wiring pattern, as required by claim 10.

Furthermore, Tada does not disclose an inspection method for inspecting a semiconductor integrated circuit using an apparatus comprising exchange boards, each electrically connecting socket terminals on the socket to a specific relay pin, as required by claim 11.

The factual determination of lack of novelty under 35 USC § 102 requires the disclosure in a single reference of each element of a claimed invention. *Electro Medical Systems S.A. v. Cooper Life Sciences Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994); *Hoover Group Inc. v. Custom Metalcraft Inc.*, 66 F.3d 299, 36 USPQ2d 1101 (Fed. Cir. 1995); *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1321 (Fed. Cir. 1987). Because Tada does not

teach an inspection apparatus for inspecting a plurality of semiconductor integrated circuits mounted on a base board, wherein the base board comprises a junction unit, wherein the junction unit includes a group of pin sockets each of which is interposed between each of a plurality of wiring patterns and a single connection terminal and/or a group of pin sockets each of which is interposed between each of a plurality of connection terminals and a single wiring pattern, and each of the pin sockets connecting the wiring pattern to the connection terminal when a pin is inserted therein, as required by claim 8; the junction unit including an element mount pattern for connecting the wiring pattern to the connection terminals when a short-circuit element is mounted on the element mount pattern and the element mount pattern is provided between each of a plurality of wiring patterns in a single connection terminal and/or between each of a plurality of connection terminals in a single wiring pattern, as required by claim 9; the junction unit including one of a dip switch for switching a junction between each of a plurality of wiring patterns and a single connection terminal and a dip switch for switching a junction between a plurality of connection terminals and a single wiring pattern, as required by claim 10; and an inspection method for inspecting a semiconductor integrated circuit using an inspection apparatus including exchange boards, each electrically connecting socket terminals of socket to a specific relay pin, as required by claim 11; Tada does not anticipate claims 8-11.

Claim Rejections Under 35 USC § 103(a)

Claims 1-6 are rejected under 35 USC § 103(a) as being unpatentable over Tada et al. in view of Chiba (U.S. Patent No. 6,100,585). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison of the invention as claimed with the cited prior art.

An aspect of the invention, per claim 1, is an inspection apparatus for inspecting a plurality of semiconductor integrated circuits mounted on a base board. The apparatus comprises a plurality of relay pins electrically connected to a wiring pattern laid on the base board, and sockets provided on the base board, each housing a semiconductor integrated circuit. The apparatus further comprises exchange boards, each electrically connecting socket terminals of a socket to a specific relay pin, and spacers interposed between each of the exchange boards and the base board.

The Examiner asserts that Tada discloses an inspection apparatus for inspecting a plurality of semiconductor IC mounted on base board including a plurality of relay pins (R1, R2) electrically connected to a wiring pattern laid on the base board (4) and sockets (2). The Examiner avers that Tada is silent concerning the exchange boards. The Examiner relies on Chiba to teach the exchange boards (15) electrically connecting socket terminals (15a) of a socket to specific relay pins (16a). The Examiner considers the spacers (16a) to also function as the spacers. The Examiner concludes that it would have been obvious "to provide the exchange board and spacer interposed within the socket mounted device for the purpose of ensuring the wiring pattern connected to socket pins to be lead onto the relay socket in its externally exposed area."

Tada and Chiba, whether taken alone or in combination fail to suggest the claimed inspection apparatus. Tada teaches a self-contained testing apparatus that has no need for additional elements, such as an exchange board and spacers. There is no indication in Tada that the apparatus of Tada would benefit by including an exchange board and spacers. Furthermore, there is no teaching in Chiba to suggest the asserted exchange board and spacers of Chiba would somehow be beneficial to the apparatus of Tada. There is no

motivation to include additional elements in the apparatus of Tada. Including additional elements in the apparatus of Tada, would make the inspection apparatus more complex for no beneficial reason. The asserted exchange boards and spacers of Chiba would not serve any useful purpose in the apparatus of Tada, and would only add to the complexity of the Tada device.

Obviousness can be established only by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion or motivation found in the teaching of Chiba to modify the teaching of Tada. The section 103 rejection is improper and should be withdrawn.

Furthermore, although a reference can be modified the prior art must suggest the desirability of modifying a reference. See *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). The Examiner's conclusion that it would have been obvious to substitute the teachings of Chiba into Tada is not supported by cited references. It appears the Examiner relied on impermissible hindsight reasoning in reaching the conclusion of obviousness.

In view of the above remarks, Applicants submit that this application is in condition for allowance and the case should be passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this

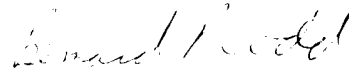
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paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. This attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at line 17 of page 11 has been amended as follows:

Further, in the structure of the burn-in board 12 according to the present embodiment, a space is ensured between the burn-in board 12 and the exchange board [20] 22 by means of the spacers [22] 20. Providing a bypass capacitor on a power line pattern or a GND pattern is effective for eliminating noise which would otherwise be superimposed on the power line pattern or the GND pattern. According to the present embodiment, a bypass capacitor can be placed in the space defined between the burn-in board 12 and the exchange board 22. In this respect, the structure of the burn-in board 12 according to the present embodiment is effective for diminishing noise which arises in an inspection process and for improving inspection accuracy.

The paragraph beginning at line 29 of page 11 has been amended as follows:

In the present embodiment, connection between the relay pin 18 and the burn-in board 12, connection between the relay pin 18 and the exchange board 22, and connection between the exchange board [14] 22 and the socket terminals 24 are realized by means of soldering. However, these connections are not limited to soldering. For instance, pin sockets may be used for holding the relay pins 18 or the socket terminals 24.

IN THE CLAIMS:

Claim 7 has been cancelled.

Claims 8, 9, and 10 have been amended as follows.

8. (Amended) [The] An inspection apparatus [according to claim 7] for inspecting a plurality of semiconductor integrated circuits mounted on a base board, wherein the base board comprises:

a plurality of connection terminals electrically connected to terminals of an inspection main unit;

a plurality of wiring patterns connected to terminals of a semiconductor integrated circuit; and

a junction unit for changing the state of a junction formed between the connection terminals and the wiring pattern, wherein the junction unit includes [a pin socket for connecting the wiring pattern to the connection terminals when a pin is inserted into the pin socket, and the pin socket] a group of pin sockets each of which is interposed between each of a plurality of wiring patterns and a single connection terminal and/or a group of pin sockets each of which is interposed between each of a plurality of connection terminals and a single wiring pattern, each of said pin sockets connecting the wiring pattern to the connection terminal when a pin is inserted therein.

9. (Amended) [The] An inspection apparatus [according to claim 7] for inspecting a plurality of semiconductor integrated circuits mounted on a base board, wherein the base board comprises:

a plurality of connection terminals electrically connected to terminals of an inspection main unit;

a plurality of wiring patterns connected to terminals of a semiconductor integrated circuit; and

a junction unit for changing the state of a junction formed between the connection terminals and the wiring pattern, wherein the junction unit includes an element mount pattern for connecting the wiring pattern to the connection terminals when a short-circuit element is mounted on the element mount pattern, and the element mount pattern is provided between each of a plurality of wiring patterns and a single connection terminal and/or between each of a plurality of connection terminals and a single wiring pattern.

10. (Amended) [The] An inspection apparatus [according to claim 7] for inspecting a plurality of semiconductor integrated circuits mounted on a base board, wherein the base board comprises:

a plurality of connection terminals electrically connected to terminals of an inspection main unit;

a plurality of wiring patterns connected to terminals of a semiconductor integrated circuit; and

a junction unit for changing the state of a junction formed between the connection terminals and the wiring pattern, wherein the junction unit includes at least one of a dip switch for switching a junction between each of a plurality of wiring patterns and a single connection terminal, and a dip switch for switching a junction between a plurality of connection terminals and a single wiring pattern.

New claim 12 has been added.